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PWM SIGNAL MEASUREMENT SYSTEM FOR QUADCOPTER AUTOPILOT AND OPERATOR RESPONSES EVALUATION

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Summary. The article deals with the design of the precise PWM signal measurement system. This system was developed using the MAX II CPLD and LPC 1768 microcontroller. 8 measurement channels were implemented into the CPLD, which makes this system suitable for the evaluation of the servo signals on a UAV quadcopter. The measurement channels can measure the PWM signals with the frequency from 5 Hz to 1 kHz while the LSB has the value of 20 ns. The system is designed in such way that it can be used for the practical measurements of the servo signals from the UAV RC receivers, UAV autopilot responses to the input signals and it can also serve as the source of information of the UAV operator reactions in the control system during their training.

Keywords: pulse-width modulation, signal parameters measurement, multichannel measurement system, quadcopter

1. INTRODUCTION

The multirotor UAVs represent nowadays commonly available aerial vehicles, which are used not only as models for hobby purposes, but they have found their application possibilities also in the civil applications as photography, photogrammetry, aerial monitoring, payload transportation etc. [1-3].

The affordably priced quadcopters are usually equipped with one of the autopilot types, e.g. ArduPilot, that is relatively wide spread. It uses the PWM (Pulse-Width Modulation) signals for the ESC (Electronic Speed Controller) control. The RC receiver outputs to the autopilot inputs the PWM signals with the repeating frequency of (approximately) 50 Hz. The signals of channels are shifted in time and the pulse width is usually from 1 to 2 ms (Fig. 1). At the autopilot output can be also regulation loop signals with higher frequencies, e. g. over 400 Hz. That is the reason why for the correct setting and testing of the navigation and regulation algorithms of the autopilot [4-6] it is convenient to create a system, which is able to record and visualise the PWM data in the real time.

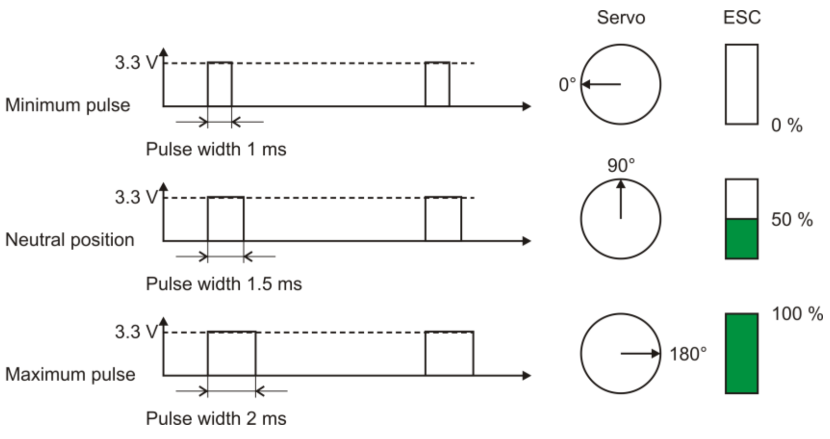

Figure 1 Servo signals

2. CPLD-BASED PWM MEASUREMENT SYSTEM

By the measurement system design it was necessary to regard several basic requirements:

- the system has to be able to measure the pulse time and the gap (space) time of the PWM signal,
- the system has to measure several channels simultaneously,
- the system has to be able to evaluate signals with different PWM frequencies,
- the system has to work with the logical levels of the LVCMOS33 (3.3 V) standard.

After the consideration of the above-mentioned requirements and availability the following hardware was chosen: MAX II CPLD (Complex Programmable Logic Device) manufactured by Altera company (the Terasic Max II Micro Kit prototyping board) and the microcontroller platform with the NXP LPC 1768 processor with Cortex-M3 core. They were integrated to create one compact device with the block diagram shown in Fig. 2. As the measurement method the direct measurement of the pulse time and of the gap time was chosen; the PWM period is evaluated as the sum of these two times. Considering the transmission of the measured data the chosen methodology offers sufficient time intervals for the data transmission from the CPLD to the master system and to the PC.

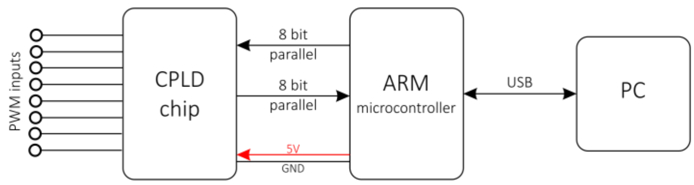

Figure 2 Block diagram of measurement system

Due to the stable and fast architecture the MAX II is able to work on high frequencies up to the 304 MHz (the maximum frequency depends on the implemented logic structure). It is compatible with the supply voltage of 3.3 V, 2.5 V and 1.8 V and the input-output interface with the logic levels of 1.5 V, 1.8 V, 2.5 V and 3.3 V. The technical specifications of the MAX II chip of the EPM2210F324C3N type are summarized in the Tab. 1.

Table 1 CPLD characteristics

Characteristics	**EPM2210**
Number of logic elements	2210
Equivalent macrocells	1700
User flash memory size (bit)	8192
Maximum user I/O pins	272
Propagation delay (ns)	7
Maximum frequency (MHz)	304
Delay time (ns)	1.2

The EPM2210 is the "biggest" chip of the MAX II family; it has 2210 logic elements. For the application in the measurement system of the PWM signal is the higher amount of elements convenient because it is possible to create more independent measurement channels on a single chip. For the measurement purposes, it was necessary to create 8 measurement channels.

The smallest structural element of the MAX II CPLD chip is one logic element, which is a small logic unit providing effective implementation of user logic functions. The logic elements are then interconnected to the blocks of logical elements, in case of the chosen chip there are ten of them in one block. These blocks are spread in the chip two-dimensionally and are ordered into columns and rows.

Among them so called MultiTrack Interconnects are realized, which provide quick and granular time delays that are much faster than the global interconnection network. Also four independent networks of the clock signals providing clock pulses for all of the components are passing through the device. They can be used also for the clear, preset and enable functions.

For the design of the implemented digital circuits the VHDL language allowing the behavioural description of the logic elements solution was used. The block diagram of one implemented measurement system channel is shown in Fig. 3. The measurement channel includes these main parts:

- input logic,
- control logic of counters,
- counters for pulse and gap measurements,
- registers.

The main task of the input logic circuitry is modification and resampling of the PWM signals because the CPLD is a synchronous device. For this purpose the couple of the D flip-flops with the same clock frequency as counters are used and so the PWM signal and the rising edge of the clock signal come to the input simultaneously. In addition to the D circuits also the PWM input, which is connected with the pull-up resistor and uses the Schmitt-trigger can supress the signal noise.

The main counters used for the PWM signal pulse or gap width measurement are 24-bit binary synchronous counters with asynchronous enable and reset. Similar counters are used in the delay blocks in the 4-bit version.

The control circuits serve for the initialisation of the register transcription after the end of the PWM pulse and for the delayed counter clearing. They consist of the D flip-flop and of the delay block. To the clock input of the D circuit the inverted PWM signal is connected instead of the clock signal and the D input connects to logical 1. So in the moment of the PWM signal pulse end the D circuit is switched and on the output occurs positive logic value, which subsequently initiates the 4-bit counter in the delay block.

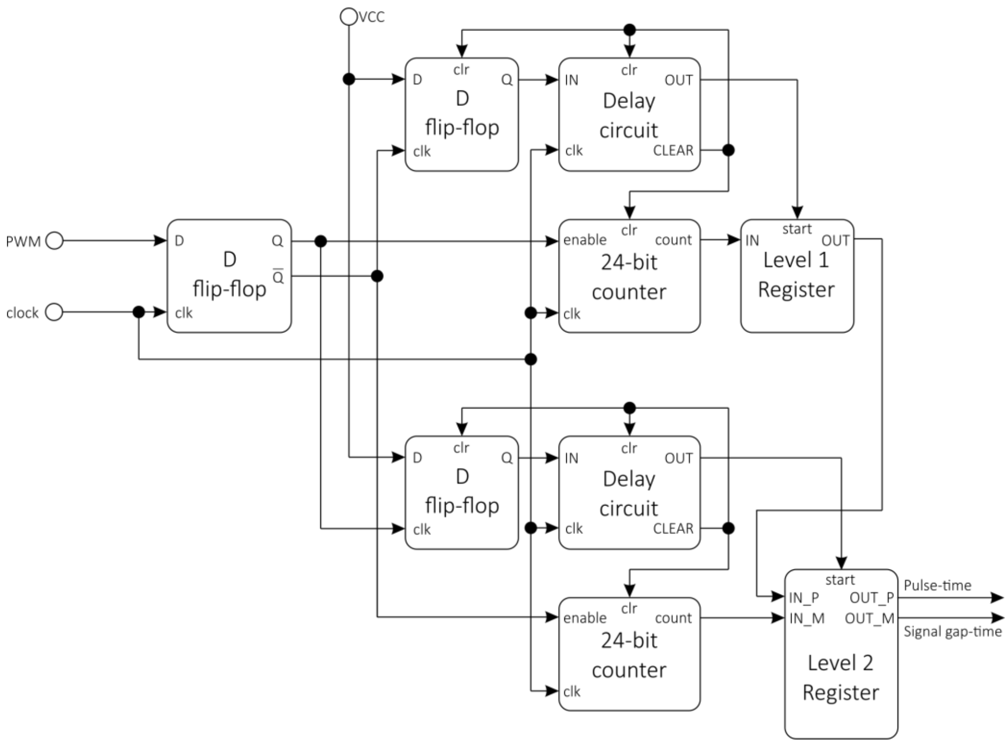

Figure 3 Block diagram of one measurement channel

The output of the delay circuit initiates the data sample write to the register. The CLEAR output clears the counter and resets all control circuits. The logic level of this output is positive, if the counter of the delay block achieves the 1011 binary value (the delay of 11 clock pulses). This timing of the output control signals provides the convenient time interval between the data writing and the counter clearing.

For the short-term data hold are used two registers on one measurement channel (one for each counter) and one common clocked register, into which all controlled registers of the measurement channels are connected.

The primary registers are controlled by the input signals of the control circuits of the pulse and gap counters. In one measurement channel two different types are used: the first degree and the second degree registers. The first-degree register is connected to the counter of the pulse width and holds the data until the end of the next pulse. It is controlled by the execute signal from the control circuit of the pulse counter. To the second-degree register inputs are connected directly the outputs of the gap time counter and the output of the first-degree register. It is controlled from the control block of the gap width counter and its outputs are lead directly to the common clocked register of the measurement system. This connection ensures that on the output of the measurement channel the pulse and gap width values of the same period are always held. To this register block is input also the signal of the PWM input disconnection.

Connection or disconnection of the inputs (on running system) by the mechanical components (by either switches or by the connecting or disconnecting of the device) generates fast transients of the input signal. To this phenomenon also contributes the fact that measurement system inputs are configured with the pull-up resistors and so by the input signal disconnection the value will obtain the logic 1 and when this logic value gets to the measurement channel, it initiates the overwrite of the register.

To supress the invalid output data from the register the disconnecting block was implemented. It is a simple counter, which has one more bit in the width in comparison to the measurement channel counters (in our case their width is 24 bits). This additional bit fulfils two tasks: it serves as a control signal for the output register of the measurement channel and in the inverted form it serves as the enable feedback for the counter itself. The inverted PWM signal inputs to the clear input of the disconnecting block counter.

If the PWM signal has in the measurement channel input the logic value equal to 0, the disconnecting block counter is cleared and maintained in this state. The disconnecting block counter begins to work (synchronously with the measurement channel pulse counter) when the input logic value is positive and it counts until the 25th bit has the logic value of 1 - in this moment the counter of the measurement channel overflows and it does not have a valid value. The signal from this bit stops the disconnecting block counter and sets up all outputs of the second-degree register of the measurement channel to 0. The disconnecting block (and also the register) remains in this state until the measurement channel input value has again the logic value equal to 0. At that time its counter is cleared and the blocking of the second-degree register output is stopped.

In Fig. 4 the simplified block diagram of an *n*-channel PWM measurement system is shown. For more channels it is necessary only to add more measurement blocks and inputs to the communication module (channels are replicated). In our case 8 measurement channels together with other circuits necessary to the required work of the measurement system were implemented. The clocked register works with the clock signal with the frequency of 1 kHz, the clock signal is lead also to one CPLD output for the communication clocking.

The communication module is the only non-autonomous block of the measurement system because it is controlled by the second superior system (the NXP LPC 1768 microcontroller) using the 8-bit code received in parallel via 8 inputs. This module is not dependent on any clock signal and reacts on the demands of the master system in real time. It works based on the demand for the exactly given 8-bit data segment of the given channel according to the coding Table 2. First two bits of the code (ID block) are reserved for the future utilization for the connection of multiple measurement systems to one common bus.

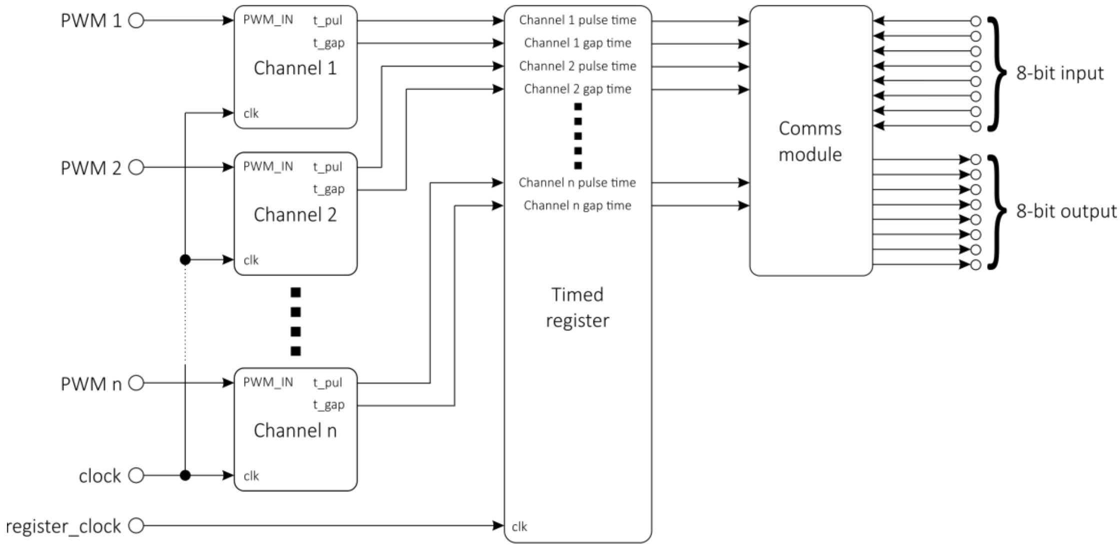

Figure 4 Block diagram of multichannel system

For the purposes of the correct system function testing without the need of the external PWM source simple generator of the test PWM signal with two outputs with the pulse width of 50 % and frequencies of 100 Hz and 1 kHz was implemented. In term of the structure it is a simple divider of the clock signal, which in the appropriate way slows the input 50 MHz clock signal to achieve required frequencies in the output.

Table 2 Communication coding table

2-bit block ID		**3-bit channel ID**		**3-bit segment ID**	
00	Block No. 1	000	Channel 1	000	Pulse: first segment
01	Block No. 2	001	Channel 2	001	Pulse: second segment
10	Block No. 3	010	Channel 3	011	Pulse: third segment
11	Block No. 4	011	Channel 4	010	Gap: first segment
		100	Channel 5	110	Gap: second segment
		101	Channel 6	111	Gap: third segment
		110	Channel 7	101	Unused
		111	Channel 8	100	Unused

The described 8-channel system with the detection of disconnected inputs, the block of the common clocking registers, the communication module and with the simple PWM signal generator uses more than 95 % of the MAX II EPM2210 chip capacity and the maximum frequencies are summarized in the Table 3.

Table 3 Maximum and used frequencies

Maximum frequencies:	
clock	103.72 MHz
register_clock	192.83 MHz
Used frequencies:	
clock	50 MHz
register_clock	100 kHz

As the master system to the CPLD the NXP LPC 1768 microcontroller platform was used. This device uses the 32-bit ARM Cortex-M3 processor core, which operates on 96 MHz. The microcontroller has 512 KB flash memory, 32 KB RAM and multiple various interfaces such as Ethernet, USB, CAN, SPI, I2C, ADC, DAC and PWM.

Basic initialization is performed and the transfer rate of the USB connection to the 960800 baud/s is set after the microcontroller start-up. The presentation of the measured data is solved by the terminal, for which the commands are given by the microcontroller through the USB connection. A complete GUI (Graphical User Interface) for the measured data visualisation will be created in the near future. Currently the following displaying modes are supported:

- A mode: The main information mode of the system, where data are ordered into the table. The data such as frequency, duty cycle and raw data from the measurement channel are printed. At the right side of the table also keyboard commands for the microcontroller control are printed.
- B mode: "Long format data stream", where the frequencies and pulse widths of all channels data in the rows together with their designations and quantities are printed.
- C mode: "Raw data stream". Only raw data of the pulse and gap width are printed.
- D mode: "Short format data stream". Only computed duty cycle data in percents are printed.
- E mode: In this mode values of pulse and gap width in nanoseconds are printed.
- F mode: In this mode values of pulse and gap width in microseconds are printed.

For illustration in Fig. 5 the created device and A mode is shown.

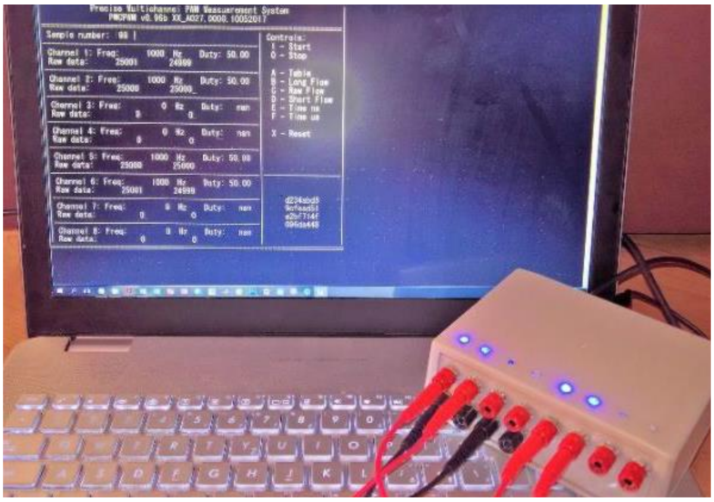

Figure 5 Created system and basic screen identic with A mode

3. INITIAL TEST MEASUREMENTS

For the verification of the correct function of the measurement system two initial test measurements were performed:

- Measurement of the transfer and frequency characteristics of the measurement system in the frequency range from 10 Hz to 1 kHz and the pulse width from 10 to 90 %.
- Test measurement of the output signals from the RC receiver.

For the measurement of the characteristics the Agilent 33521A function generator and the frequencies of 10 Hz, 50 Hz, 100 Hz, 200 Hz, 500 Hz and 1000 Hz were used. The signal duty cycle was stepwise changed from 10 to 90 % with the step of 10 %. For each value 1000 samples were recorded. Based on the measured data the transfer and frequency characteristics of the measured signal pulse time and duty cycles were created (Fig. 6 - 8).

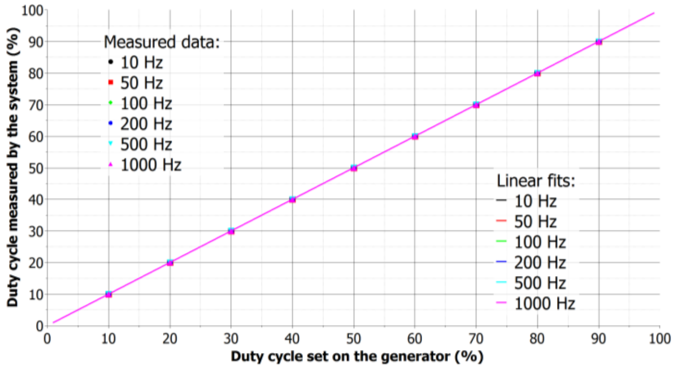

Figure 6 Transfer characteristics for various frequencies of the input signal

From the measured dependencies it can be seen that the created measurement system is able to measure consistently in the whole specified measurement range from the signal frequency and also duty cycle point of view. The system shows similar values of the measured data for the whole frequency range from 10 Hz to 1000 Hz without the indication of the measurement error even on the boundary frequencies.

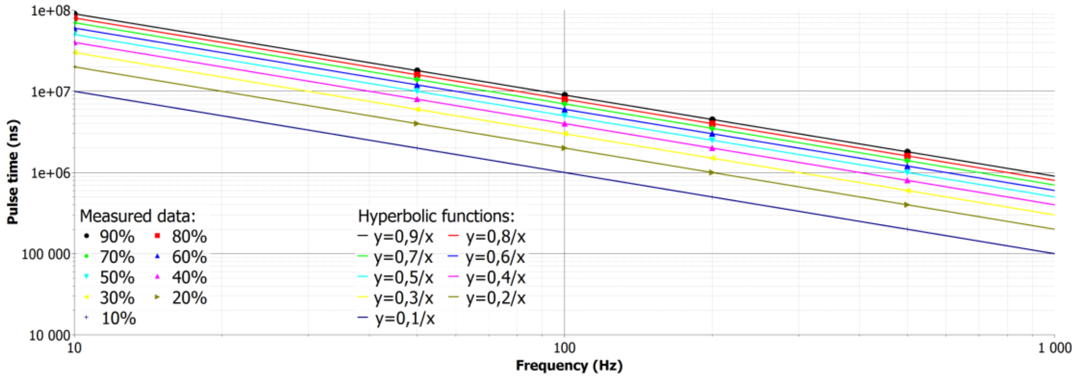

Figure 7 Frequency dependencies of the pulse times for different pulse widths

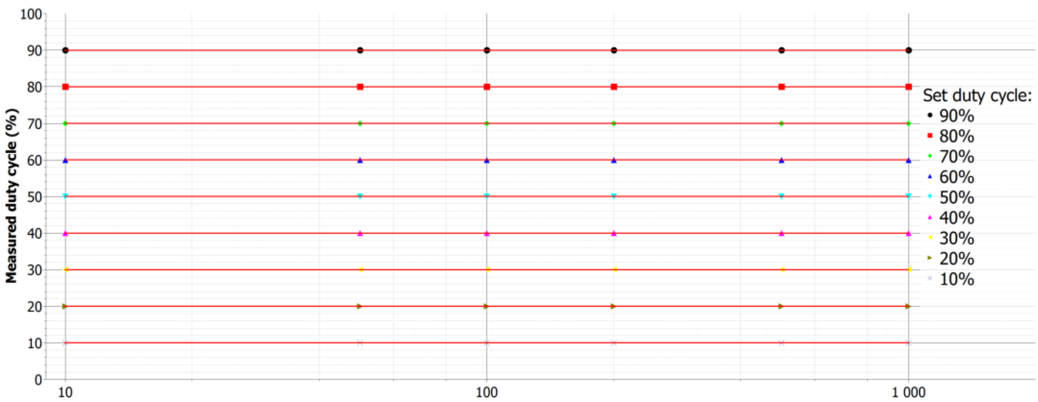

Figure 8 Frequency characteristics of the measurement system

During the next measurement the created system was connected to the outputs of the Orange RX R615 RC receiver consequently to the throttle (THRO), rudder (RUDD), elevator (ELEV) and ailerons (AILE) output channels. As the source of the control signal the Spektrum DX7 RC set was used. In every channel 5 positions (0 %, 25 %, 50 %, 75 % and 100 %) of the transmitter sticks were measured. Each measurement run 10 s, during which 10000 samples in the specified position of the steering arm of the given channel were measured. Due to the similarity of the signals for the illustration only some of the THRO channel measurements are shown in Fig. 9. Measured signal data are summarized in Table 4. From the measurement results the transfer characteristics of the RC set – RC receiver chain was obtained (Fig. 10, Table 5). From the results it can be seen, that the channels differ slightly.

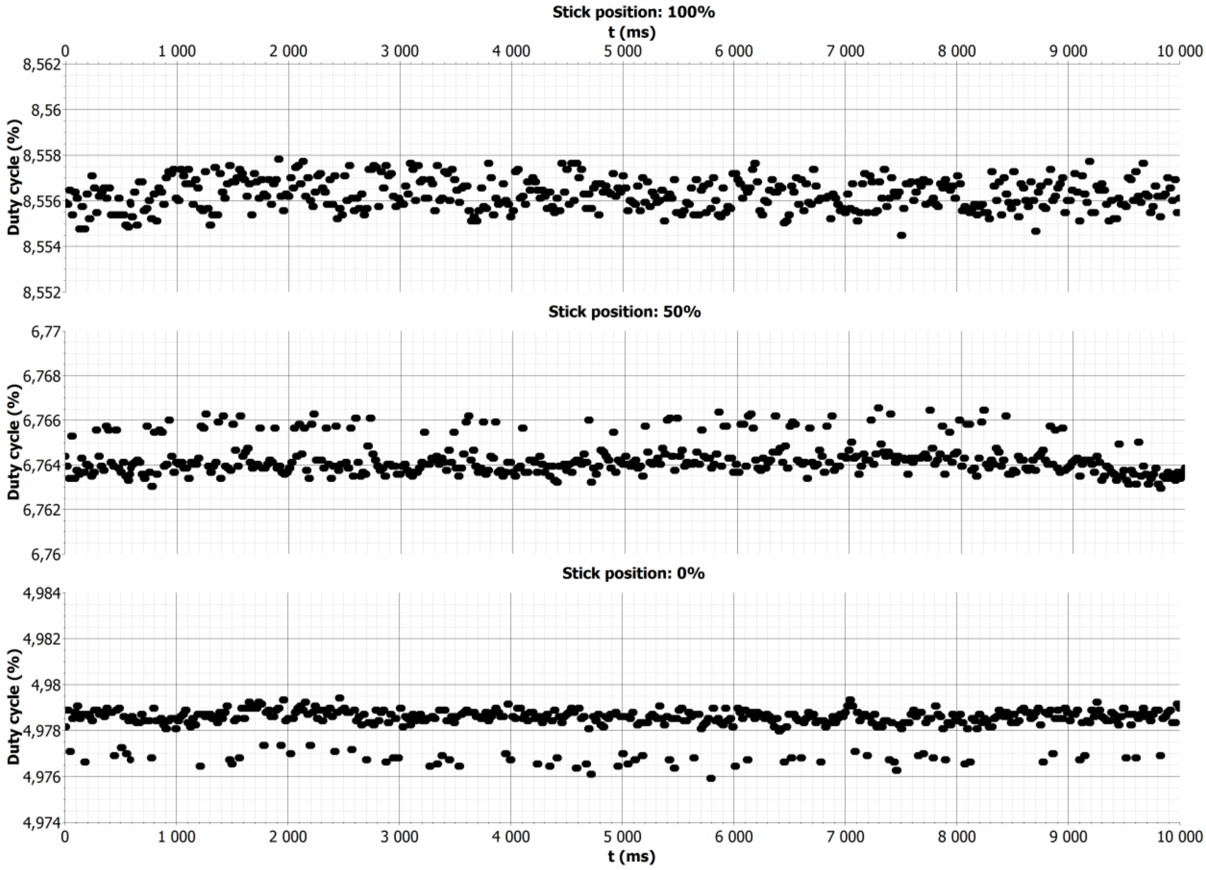

Figure 9 THRO channel output signals

Table 4 Measured signal data

Pos.	THRO					RUDD				
[%]	**AVG [ns]**	**STDEV**	**MIN**	**MAX**	**u_a**	**AVG [ns]**	**STDEV**	**MIN**	**MAX**	**u_a**
0	1106311.18	154.57	1105760	1106580	0.119	1103286.01	261.18	1102740	1103700	0.154
25	1296200.41	138.29	1295920	1296520	0.112	1301059.85	249.12	1300600	1301480	0.150
50	1503171.07	174.41	1502820	1503680	0.126	1507123.13	235.78	1506520	1507580	0.146
75	1707089.85	263.60	1706540	1707660	0.155	1717926.86	218.65	1717280	1718280	0.141
100	1901402.46	151.22	1901000	1901760	0.117	1904119.44	278.95	1903580	1904700	0.159
Pos.	**ELEV**					**AILE**				
[%]	**AVG [ns]**	**STDEV**	**MIN**	**MAX**	**u_a**	**AVG [ns]**	**STDEV**	**MIN**	**MAX**	**u_a**
0	1100965.85	136.52	1100660	1101220	0.111	1104257.41	216.82	1103880	1104620	0.140
25	1289538.51	82.95	1289340	1289840	0.087	1293036.01	301.42	1292380	1293400	0.166
50	1496638.13	215.97	1496200	1497280	0.140	1502595.90	333.30	1502100	1503180	0.174
75	1722631.89	216.09	1722200	1723300	0.140	1714529.75	342.92	1713980	1715160	0.177
100	1906467.38	221.10	1905960	1907080	0.142	1905283.62	237.59	1904800	1905800	0.147

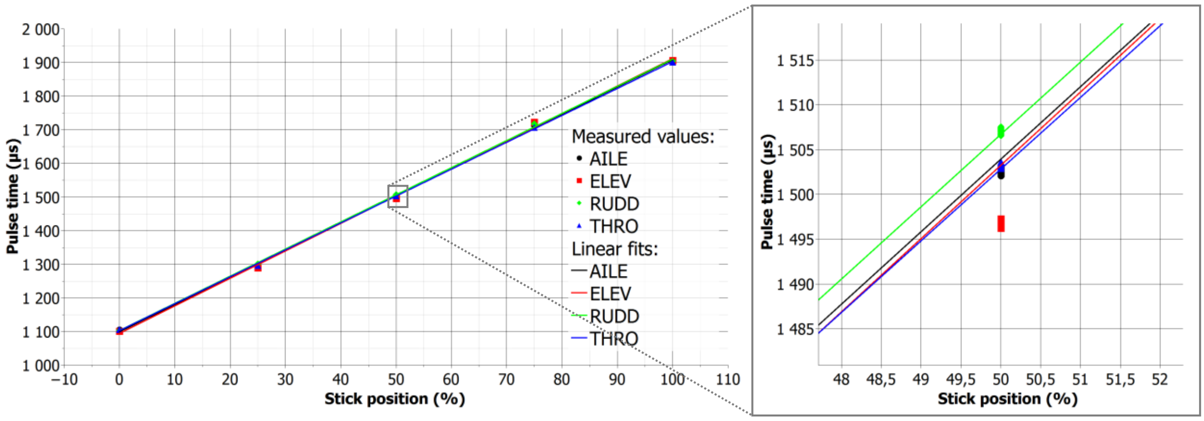

Figure 10 Transfer characteristics of the RC set – RC receiver chain

Table 5 Linear fit coefficients

y = Ax + B	AILE	ELEV	RUDD	THRO
A	8.09	8.18	8.07	8.00
B	1099.23	1094.43	1103.00	1102.62

4. CONCLUSION

The created PWM system measurement consists of 8 measurement channels operating simultaneously, the control signals generator and the logic for the clearing of the register output data in case of the absenting PWM signal in the outputs. For the PWM signal measurement is used the direct measurement of the pulse and gap time measurement, the PWM period is evaluated as the sum of these two time intervals. The chosen method offers sufficiently long time intervals for the data transmission to the master system and to the PC, since the system is able to work with the PWM frequency of 1 kHz and by the utilization of 8 channels the data rate is relatively high. The system can operate in several modes according to the user demands. By the chosen 24-bit width of the counters it is able to measure the PWM signals with the frequencies from 5 Hz up to the 1 kHz, whereby it is theoretically able to measure up to the hundreds of kHz. For the counter clocking the clock oscillator with the frequency of 50 MHz was used, which means that one LSB of the counter means 20 ns. The system is USB-powered and can be used basically with every PC.

Initial test measurements proved the correct system function. The system is designed so that it can be used for the purposes of practical measurements in various applications, mainly for the measurements of the UAV RC receivers, UAV autopilot responses to the input signals and last but not least by the UAV operators' training as the source of the information about their reactions in the control system [7][8].

By the quadcopters all eight channels of the measurement system can be used - four channels can be connected between the receiver and autopilot and the next four channels between the autopilot and the electronic regulator of the electromotor. So it is possible to monitor the UAV autopilot and also operator reactions in the real time.

Acknowledgement

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